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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/658,597	09/11/2000	Steven P. Larky	0325.00418 CD117	4974

21363 7590 12/02/2002

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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/658,597	Applicant(s) LARKY ET AL.
	Examiner Jeffrey R. West	Art Unit 2857

-- Th MAILING DATE of this communication appears on th cover sheet with th correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 1, lines 1-2, "The present application may relate" should be --- The present application relates---.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-8, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,784,581 to Hannah in view of U.S. Patent No. 6,345,373 to Chakradhar et al.

Hannah discloses an apparatus and method for operating a Universal Serial Bus (USB) peripheral device as either a master or a slave to permit communication between the USB device and other connected USB devices without requiring an active host controller (column 3, lines 3-13) by providing a peripheral device capable of detecting when there is no host controller present and, when no host controller is detected, emulating the host (column

4, lines 11-14) to issue commands and tokens to control the operation of the other peripherals interfaced to the host emulator (column 4, lines 58-63).

Hannah, however, discloses supplying commands or tokens to the USB devices instead of applying testing commands and also does not teach an apparatus to configure a low speed tester to conduct high-speed tests.

Chakradhar teaches an apparatus (i.e. a test generator), coupled to a circuit under test and a low speed tester, that generates a plurality of test vectors to allow at-speed (column 12, lines 32-33) testing of VLSI circuits at a high speed using the low speed tester (column 8, lines 51-60 and Figure 10) wherein the generation of the test vectors depends on the speed of the slow tester (column 9, lines 10-13). Chakradhar also discloses testing the circuit device by examining the input reception and output transmission of the vectors (column 10, lines 33-49).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hannah to include applying testing commands using an apparatus for configuring a low-speed tester to conduct high-speed tests, as taught by Chakradhar, since Hannah is silent on the type of commands the master device executes and the combination would have provided a method for insuring accurate operation of the USB system in a way that, as suggested by Chakradhar, would have increased the fault coverage and reduced the application time (column 12, lines 40-42) without extra costs of providing a high-speed tester. Further, since Chakradhar teaches controlling the test generator with the low speed tester (column 9, lines 34-37), it would have

been obvious to one having ordinary skill in the art to include controlling the host emulator with the low speed tester because the host emulator is acting as the test generator.

4. Claims 2 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hannah in view of Chakradhar, and further in view of U.S. Patent No. 6,343,260 to Chew.

As noted above, Hannah and Chakradhar teach many of the features of the claimed invention, including a USB system device capable of receiving commands as a slave device and transmitting commands as a master device (Hannah, column 5, lines 16-30) and re-transmitting the received data to another connected USB device (Hannah, column 3, lines 32-47), but do not teach a method for verifying the device under test during testing or that the test device generate a test packet to be executed.

Chew teaches a universal serial bus test system comprising a USB, a USB host controller coupled to the USB, and a set of USB interfaces which allow communication between a test application and a host controller driver, wherein the test application is configured to examine USB device descriptors and construct corresponding state information for the devices (column 3, lines 47-57). Chew also teaches connecting a plurality of peripheral devices to the USB port (column 4, lines 23-26) and that the testing apparatus (i.e. host device) initiates test data packets (column 5, line 67 to column 6, line 6), including a test application (column 6, lines 53-56), or a suite of tests, to be

sent to the USB test device for reception and verification that the USB device can provide appropriate device information (column 7, lines 24-27).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hannah and Chakradhar to include a method for verifying the device under test during testing and specifying that the test device generate a test packet to be executed, as taught by Chew, because the combination would have provided the necessary complex test instructions needed to perform thorough testing and, as suggested by Chew, provided fast responses to user requests as well as insured that the USB devices connected to the USB behave as required by the USB Specification (column 3, lines 58-65).

5. Claims 13, 14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hannah in view of Chakradhar, and further in view of U.S. Patent No. 6,002,868 to Jenkins et al. and U.S. Patent Application Publication No. 2002/0011516-A1 to Lee.

As noted above, Hannah and Chakradhar teach all of the features of the claimed invention except for providing that the tester generate a pass/fail signal and that the apparatus is configured to perform at least one test of a plurality of USB 2.0 test modes for use in a production test environment.

Jenkins teaches a test definition tool for the diagnosis of machines in a factory environment (column 2, lines 14-16) wherein a test dispatcher module monitors the testing of a plurality of hardware devices including a USB (Table

3) and builds an array of records including whether the current test is running, the percentage of the test that is complete, and the pass/fail status of the test (Table 2). Jenkins also teaches implementing a test selection phase to select between quick, complete, custom, interactive, or unattended test modes (column 11, lines 54-61).

Lee teaches a smart card virtual hub for use in a manufacturing environment (paragraph 0018) comprising a USB bus that supports data exchange between a host computer and a wide range of simultaneously accessible peripherals (paragraph 0033) wherein the peripherals are slaves that obey a defined protocol and react to request transactions, including device details and configuration, sent from the host control (paragraph 0049). Lee also teaches that the system is operated over USB 2.0 (paragraph 0050) to control the port enable, disable, and suspend modes (paragraph 0082) as well as the full speed or low speed of the signals (paragraph 0081).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hannah and Chakradhar to include providing that the tester generate a pass/fail signal and that the apparatus is configured to perform at least one test of a plurality of USB 2.0 test modes for use in a production test environment, as taught by Jenkins and Lee, because the combination would have provided a means for conveying the result of the test to indicate to the user whether the devices are in correct operable condition, allowed for increased user control of the test based on time constraints or user intervention availability, and, as suggested by Lee, allowed for the testing of

higher speed devices because USB 2.0 operates at a faster speed (paragraph 0050).

Response to Arguments

6. Applicant's arguments filed 09 September 2002 have been fully considered but they are not persuasive.

Applicant first argues that the combination of Hannah and Chakradhar does not teach the feature of "an apparatus coupled to a low speed tester and a device" and "high speed tests of the device through an apparatus/testing means/host emulator" because Figure 10 of Chakradhar "shows that the test generator (USB master device) does not interface with the tested circuit 10.2 (USB slave device)". The Examiner maintains, however, that since the test generator generates the test vectors based on continuously observed speed limitations of the slow tester (i.e. changing input values) (column 9, lines 10-13 and column 10, lines 17-32), the slow tester must interface with the test generator and, in order to transmit the generated test vectors to the device under test, must also interface with the device under test.

Applicant then argues "if the USB master device of Hannah is the input vector block 10.3 of Chakradhar, then the input vector block 10.3 would have bi-directional interfaces to (i) the tested circuit 10.2 and (ii) to the slow tester 10.1 to support the master/slave bus traffic contrary to the unidirectional interfaces taught by Chakradhar". The Examiner maintains, however, that the invention Hannah is being modified by the invention of Chakradhar to include

the specifics of the high speed testing therefore the interfaces of Chakradhar would not be modified in the combination of the two references.

Applicant then argues that there is no motivation to combine the inventions of Hannah and Chakradhar because Hannah appears silent on testing devices and "there is no motivation or suggestion by Hannah to seek the teaching of Chakradhar to implement an apparatus or low speed tester for such tests." The Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art (See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992)), but it is not necessary to specifically find motivation for modifying the primary reference in the primary reference itself. The Examiner contends that motivation still exists to combine the two references because the combination would have provided a method for insuring accurate operation of the USB system in a way that, as suggested by Chakradhar, would have increased the fault coverage and reduced the application time (column 12, lines 40-42) without extra costs of providing a high-speed tester.

Applicant then argues that while "Chakradhar may suggest testing of the combined master/slave system taught by Hannah as the tested circuit 10.2, but not testing of just the slave device remotely through the master device"

and therefore Chakradhar does not appear to teach or suggest high speed tests of a device through an apparatus/testing means/host emulator as presently claimed. This feature has already been explained above. Further, the invention of Hannah teaches using one USB device emulating a host to execute commands to a peripheral interfaced to the host emulator. The combination of Hannah and Chakradhar would include the similar structure of using one USB device to test an interfaced peripheral.

Applicant then argues that "the Office Action does not provided any additional evidence that the suggested combination would be motivated or suggested by knowledge generally available to one of ordinary skill in the art" but as mentioned above the combination would have provided a method for insuring accurate operation of the USB system in a way that, as suggested by Chakradhar, would have increased the fault coverage and reduced the application time (column 12, lines 40-42) without extra costs of providing a high-speed tester

Applicant argues that "the Office Action does not provide clear and particular evidence that there is a reasonable expectation of success for the suggested combination" and "[t]he increased fault coverage and reduced application time cited in Chakradhar may apply to the configuration taught by Chakradhar, but no evidence has been provided in the Office Action that an increase fault coverage or reduced application time would be experienced in the suggested combination" specifically because in Chakradhar "the slow tester 10.1 has direct access to the tested circuit 10.2 to observe output

signals from the tested circuit 10.2" and in contrast, "modifying the master/slave system of Hannah with Chakradhar would place the master device between the slow tester 10.1 and the tested circuit 10.2". As noted above, the Examiner maintains that the invention of Chakradhar does provide testing through the test generator. Further, the invention of Chakradhar describes "the increased fault coverage and reduced application time" as a result of the vector testing method taking into account the speed of the tester rather than the specific structure of the testing circuit (column 12, lines 32-42).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications

from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
November 26, 2002

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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